Device Noise Simulation of ΔΣ Modulators

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This report describes behavioral simulation of ΔΣ analog to digital converters including the effects of device noise. Simulation of the feedback loop filters with SpectreRF provides the statistics of the device noise. A discrete time filter is used to generate noise with similar power spectral density (PSD) during the behavioral simulation. A second order converter is used to demonstrate the methodology and the simulation results are presented. Our approach does not make assumptions about the device and quantization noise adding linearly and takes into account their interaction. It is numerically efficient, as the behavioral simulation does not require significantly higher computational effort than in the case that device noise is not included. The same approach can be applied to continuous time converters.

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1 Introduction

Delta-Sigma (ΔΣ) data converters are widely used, particularly in applications where high precision is required and the signal band is relatively small, such as in the processing of audio and sensor signals. They are inherently insensitive to process imperfections such as component mismatch and they can be easily integrated in inexpensive CMOS technologies. Receiver architectures that employ band-pass ΔΣ A/D converters to replace part of the analog RF part have been proposed [4, 5].

Because ΔΣ converters are large mixed-signal circuits and their performance characterization requires extremely long transient simulations, transistor level simulation is impractical because of time limitations. Behavioral simulation is used instead to test the functionality of a design. The behavioral models of the building blocks can include second-order effects such as finite opamp gain, finite opamp slew rate, component mismatch and nonlinearities [13]. It is the subject of this study to include device noise in the behavioral models.

Although device noise is often a limiting factor in the performance of ΔΣ data converters, it is not usually taken into account in simulations. Simulating noise with a circuit simulator at the transistor level is impractical as explained above. In addition, circuit simulators that are capable of providing the noise PSD at the output of circuits with a time-varying operating point, such as the Cadence analog simulator Spectre®RF†, require a periodically changing operating point. The operating point of ΔΣ converters in general changes in a non-periodic fashion even for a DC input [1].

In this report we describe the device noise characterization of the building blocks of the converter, and the subsequent behavioral simulation. To demonstrate the proposed methodology, we use a discrete time second-order ΔΣ converter as an example. The SpectreRF analog simulator is used for characterization of the building blocks. When compared with the usual behavioral simulation of ΔΣ converters, the proposed methodology does not require more timesteps and does not significantly increase the computational effort. This is a significant advantage compared to other suggested approaches [12]. Because of the multitude of architectures used in ΔΣ converters, the designer will probably need to modify the presented methodology to fit its own needs.

2 ΔΣ AD Converter Background

The block diagram of a ΔΣ analog-to-digital converter is shown in Figure 1. It is a feedback loop that employs filters, an Analog-to-Digital Converter (ADC) and a Digital-to-Analog Converter (DAC). The resolution of the ADC and DAC is much lower than that of the ΔΣ converter. Often the ADC is a comparator and the DAC converter has only two output levels. Digital values are produced at the output of the ADC at a much higher rate than the signal bandwidth. The ΔΣ converters are oversampling converters, which means that the quantization noise power is spread over the wide sampling frequency range and only a small part of it falls in the signal band. The ratio of the sampling frequency over the Nyquist rate is called the oversampling ratio. The quantization noise in the signal band is further suppressed by the loop gain. The operation of the converter

†. Spectre is a registered trademark of Cadence Design Systems.

can be better understood from the linear loop model of Figure 2 in which the quantizer formed by the ADC and DAC of Figure 1 have been replaced by a source of quantization error e_n. The representation of Figure 2 is accurate, but one must be aware of the fact that the quantization error e_n is not an independent input, but completely determined by the input signal. Under conditions of busy input signal the quantization error values resemble uncorrelated samples with a flat frequency spectrum, and the quantization error source resembles an independent white noise source. The loop filters are such that the transfer function of the input signal x_n to the output y_n in the signal band is a constant, while the transfer function from the quantization noise source e_n to the output y_n is ideally zero. In reality, the quantization error is not white but it contains periodic patterns that give rise to tones, or spikes in the frequency spectrum. These spikes contain high energy and deteriorate the performance of the converter if they fall in the signal band. Strong quantization noise tones can be detrimental even if they are out of band, since they can leak into the signal band through intermodulation distortion, or mixing with a parasitically coupled strong clock signal [1].

FIGURE 1 *A ΔΣ analog-to-digital converter.*

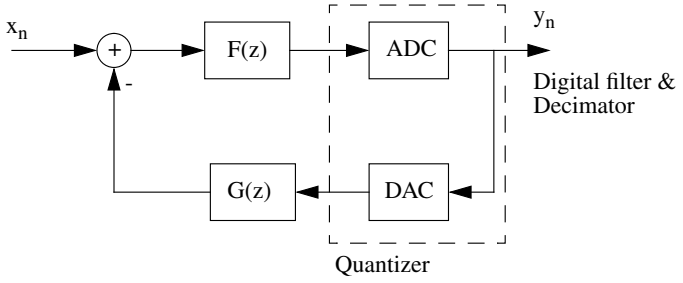
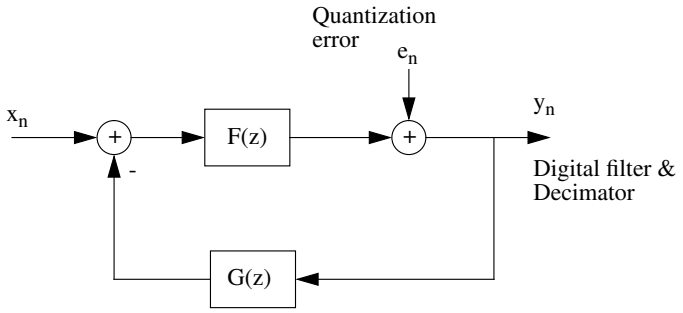


FIGURE 2 *The linearized model of a ΔΣ analog to digital converter.*



The loop filters are often discrete time switched capacitor filters, but they can also be continuous time active or passive filters, in which case the converter is called continuous time. In a baseband converter, the loop transfer function is an integrator or another low-pass filter, while in a bandpass converter the filter is a resonator.

To randomize the quantization error and avoid the generated tones, a pseudorandom signal is often added at the input of the quantizer. This technique is known as dithering [1]. It is known that the device noise also has a dithering effect, but in most cases inadequate to effectively remove completely the undesired tones [1].

The order of the delta-sigma converter is defined as the order of the loop transfer function. The higher the order the better the noise suppression, but usually designs of order higher than two are prone to instability. An alternative that effectively implements higher order noise suppression is the cascaded, or multistage, or MASH (Multistage Noise Shaping), converters. In these, the quantization error of a low order converter is processed as an input to another ΔΣ converter. Digital logic combines the outputs of all stages to one output, and ideally the resulting conversion is equivalent to that of a single stage converter of order equal to the sum of the orders of all individual stages. The proposed methodology can be used for discrete or continuous time converters, and can be adapted for cascaded converters. If dithering is employed it can be simulated simultaneously with the device noise.

3 Methodology

The analog circuitry of a ΔΣ converter contributes device noise, which together with the quantization noise, contaminates the output. In cases where in the signal band one of the two sources of noise is much lower than the other, the weak one can be neglected. If the quantization error is dominant, its effect can be simulated in the behavioral level as is commonly done with Midas [14], Matlab, a programming language such as c, or Verilog-A [7,15]. If the quantization noise is very low in the signal band as in cases where the oversampling ratio is very high and there are not tones of accumulated energy, its effect can be neglected, and the in-band device noise alone suffices to be considered. If it is known that the quantization error truly resembles white noise and that the linear model of Figure 2 holds, the output device and quantization noise can be found separately as if the other source were not present, and then added to obtain the total output noise.

In the general case however both sources of error are present and the device noise affects the quantization noise. In particular, if one source of noise is negligible, design resources have probably been wasted. In wideband applications, the oversampling ratio cannot be very high and the quantization noise cannot be arbitrarily low. The out-of-band device noise indirectly has an effect on the performance because it affects the in-band quantization noise.

Since the digital filter reads periodically the ADC output and the signal fed back through the DAC must be exactly what the digital filter reads, the ADC must be clocked with latched output, in both discrete and continuous time ΔΣ converters. Therefore, the device noise that the analog circuitry generates can be represented by a discrete time noise process injected at the input of the ADC. With the proposed methodology the combined effect of the device and quantization noise can be estimated. It can be summarized in the following steps

- The noise performance of the analog circuits involved in the loop is characterized and the PSD of the equivalent discrete time noise process at the quantizer input is determined.
- A discrete time filter is found, which when fed with white noise, generates noise with PSD similar to that of the equivalent noise.
- Time domain behavioral simulation with a representative input signal is run, similarly to how it is done for quantization noise effects in [13, 14]. In addition, noise generated by the discrete time filter is injected at the input of the ADC. The fre-

quency spectrum of the time domain output reveals the quality of the data conversion. The behavioral models used for the building blocks can be otherwise ideal, or they can include other nonidealities, as described in [13]. Dithering can also be present in the simulation.

4 Device Noise Estimation

A necessary assumption in the noise characterization of the analog part is that the generated device noise is independent of the input signal and the ADC output, which is in general a non-periodic signal. The assumption that the generated noise is independent of the input signal is usually made in the characterization of switched capacitor and continuous time active filters, similar to those used in discrete and continuous time ΔΣ converters respectively. It is usually accurate and it will be discussed in detail for the example circuit of Section 5 on page 8.

Let us consider first discrete time ΔΣ converters. The operating point of the devices in the switched capacitor filter changes wildly during the clock period. Assuming as we mentioned above that the generated device noise is independent of the processed signal, noise at the input of the ADC is a continuous time cyclostationary process $u(t)$ with PSD $S_u(f, t)$. Let t_0 denote the time instant within the clock period at which this process is sampled by the ADC, and $u_\mathrm{d}(nT_\mathrm{s})$ denote the resulting discrete-time noise process. It is intuitive and also easy to show that sampling a cyclostationary process once in a period results in a stationary discrete time process. The PSD of $u_\mathrm{d}(nT_\mathrm{s})$ is[†]

$$S_{u_\mathrm{d}}(f) = \sum_{k=-\infty}^{\infty} S_u(f - kf_\mathrm{s}, t_0) \tag{1}$$

The Cadence analog simulator SpectreRF is capable of accurately predicting the noise performance of switched capacitor circuits [8, 9]. It is a continuous time simulator and provides the time average noise PSD. To extract $S_{u_\mathrm{d}}(f)$, an ideal sample and hold circuit (S/H) can be employed, which samples the noise process $u(t)$ at time t_0 and holds this value for a whole period.[‡] Let us denote the piecewise constant output of the S/H circuit with $u_\mathrm{sh}(t)$. It can be easily shown that this is a cyclostationary process and the time average of its PSD $S_{u_\mathrm{sh}}(f)$ is related with the PSD of $u_\mathrm{d}(n)$ by

†. We are using here the following definition for $S_{u_\mathrm{d}}(f)$

$$S_{u_\mathrm{d}}(f) = T_\mathrm{s} \sum_{k=-\infty}^{\infty} R_{u_\mathrm{d}}(kT_\mathrm{s}) e^{-jk2\pi T_\mathrm{s} f}$$

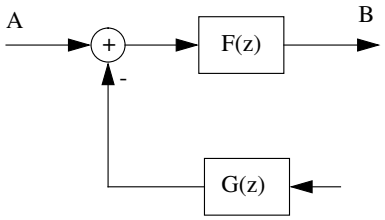
where $R_{u_\mathrm{d}}(kT_\mathrm{s})$ is the autocorrelation function of $u_\mathrm{d}(nT_\mathrm{s})$. If it is desirable to find the power of $u_\mathrm{d}(nT_\mathrm{s})$ one should integrate $S_{u_\mathrm{d}}(f)$ as given by the following equations from 0 to $f_\mathrm{s}/2$, if the PSD $S_u(f, t)$ of the continuous time processes on the other side of the equation is single sided, or from 0 to f_s if it is double sided. SpectreRF provides single-sided PSDs.

$$S_{u_{sh}}(f) = \left(\frac{\sin(\pi f T_s)}{\pi f T_s}\right)^2 S_{u_d}(f) \tag{2}$$

We intend to perform time domain behavioral simulation, during which the feedback loop will be closed through the quantizer, and $u_d(n)$ is the noise signal that we intend to add at the quantizer input. Therefore, during the simulation of the switched capacitor filter with SpectreRF that will provide $u_d(nT_s)$, the loop filter must be open as shown in Figure 3. Alternatively instead of injecting a noise signal in front of the quantizer we can inject at the input a noise signal $w(n)$ with PSD

$$S_w(f) = \frac{1}{|F(f)|^2} S_{u_d}(f)\,. \tag{3}$$

FIGURE 3 *The feedback loop open. The input of filter G(z) is zero. The noise process u(t) is the output noise at point B, while w(t) is the noise referred to point A.*



It is easy to see that the input referred noise of an open loop system is identical to the input referred noise of the closed loop system and therefore $S_w(f)$ can be also be calculated from the closed loop system of Figure 4. This is useful because, as we will see in the example of the next section, in some cases it is easier to simulate a closed loop system rather than the corresponding open loop.† In addition, SpectreRF provides directly the PSD of the discrete-time input-referred noise, and one does not need to compensate for the term $(\sin(\pi f T_s)/(\pi f T_s))^2$ as in (2). Let us denote the closed-loop output noise by $v(t)$, its sampled version by $v_d(n)$, and the output of the corresponding S/H circuit used in simulation by $v_{sh}(t)$. Similarly to (2)

$$S_{v_{sh}}(f) = \left(\frac{\sin(\pi f T_s)}{\pi f T_s}\right)^2 S_{v_d}(f)\,, \tag{4}$$

‡. Such an ideal sample and hold circuit is described by Kundert [6] and consists of a sampling capacitor in series with a time varying resistor. It does not represent a load for the sampled circuit, it has infinite driving capability and its time constant during the sampling phase can be arbitrarily small. The sampling instant is given with the delay parameter, and in our application the aperture must be much smaller than the period (such as 1/100th), and the time constant *tc* about 10 times smaller than the *aperture*.

†. When a simulation for the input-referred noise of a switched capacitor circuit is performed, it is advisable that an additional ideal S/H is used at the input, sampling the input signal anytime outside the sampling phase of the actual input S/H of the circuit, implemented with real switches. This is because the actual S/H may have adequate bandwidth for a baseband signal, but not for one close to $f_s/2$. The ideal S/H freezes the input signal and the actual S/H has enough time to settle. The input referred noise simulated in this way can then be used with the ideal transfer function in the behavioral simulation, to provide the correct output noise at all frequencies.

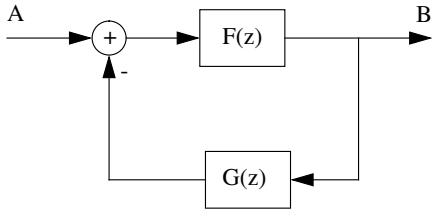
where $S_{v_{sh}}(f)$ and $S_{v_d}(f)$ are the time average of the PSD of $v_{sh}(t)$ and the PSD of $v_d(n)$ respectively. Assume that closed loop system implements the discrete time transfer function $H(f)$. In order to calculate the input referred noise, SpectreRF divides $S_{v_{sh}}(f)$ with

$$\left(\frac{\sin(\pi f T_s)}{\pi f T_s}\right)^2 |H(f)|^2 \tag{5}$$

and provides

$$S_{w_d}(f) = \frac{1}{|H(f)|^2} S_{v_d}(f) \tag{6}$$

FIGURE 4 *The closed feedback loop without the quantizer. The input referred noise w(t) is obtained at A, while the output noise v(t) is obtained at B.*



In a continuous time ΔΣ converter, the continuous time input and feedback signals are processed by the continuous time filters. However, as explained above, the ADC performs periodic discrete time comparisons and there are transformations [1] that map the continuous time converter to a discrete time one, in order to perform behavioral simulations. We can therefore apply our methodology in the same way in continuous time converters, injecting an appropriate discrete time noise signal at the input of the ADC during the behavioral simulation.

Any active circuits, such as transconductors, used in the implementation of the loop filters must operate linearly and therefore the bias current of the active devices is constant. The statistics of the device noise generated are time invariant and the noise at the input of the DAC is stationary. The corresponding PSD can be found with a time invariant noise analysis, with SPICE or SpectreRF and then folded manually to account for the sampling aliasing.

$$S_{y_d}(f) = \sum_{k=-\infty}^{\infty} S_y(f - kf_0) \tag{7}$$

An ideal S/H can be used to obtain the spectrum of the discrete time process directly from SpectreRF, using an equation similar to (2). Often in order to minimize the effect of memory from previous cycles and the jitter in the response delay of the quantizer, a return to zero sample and hold circuit is used at the DAC output [4]. In this case the noise at the ADC input is rather cyclostationary, but is transformed to a stationary discrete time noise process when it is sampled at the ADC input, whose PSD can be found in a way similar to this described for the switched capacitor circuits.

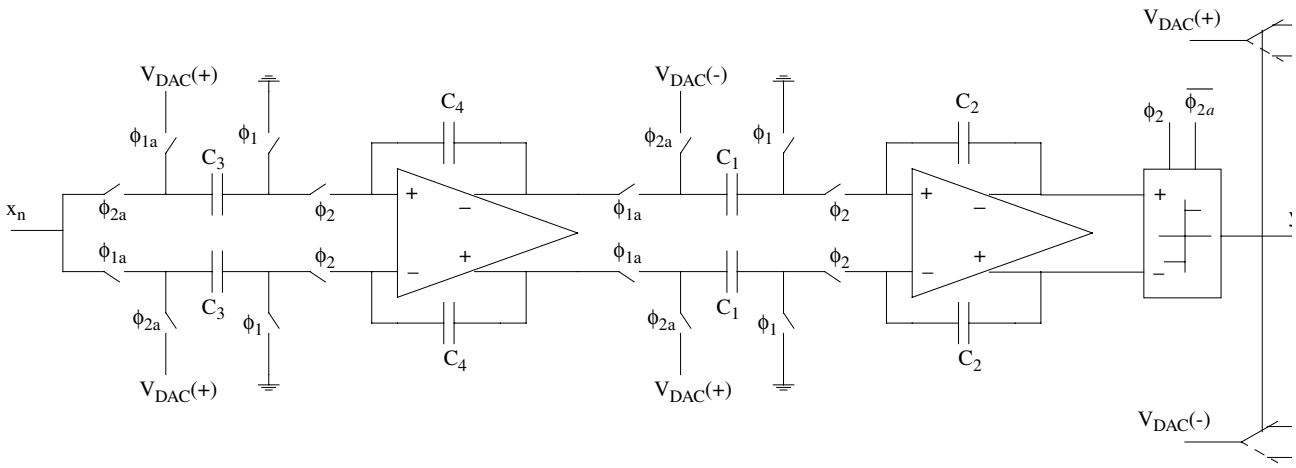
Noise and any nonideality of the ADC are rather insignificant. It is important to notice that when a wrong decision taken by the ADC and read by the digital filter, the same wrong decision is fed back to the input, and will be corrected for in the future cycles. The in-band input referred noise of the ADC gets suppressed by the feedback loop in a way similar to the quantization noise. The out-of-band noise however could have an effect on the quantization noise, but this effect is unlikely very significant.

The device noise of the DAC does not get suppressed by any mechanism has a direct effect on the in band noise and it also affects the quantization noise.

5 Example: A 2nd Order ΔΣ Converter

We will now consider practical issues in the simulation of switched capacitor filters used in ΔΣ converters. The second order converter of Figure 5 will be used as an example. It is a baseband converter and employs two switched capacitor integrators in the feedback loop. The clocks exciting the circuit are shown in Figure 6. The comparator is shown in Figure 7 in which we see that the comparisons take place at the end of ϕ_2, or 78 ns after the beginning of the period.† An approximate noise analysis of such a circuit is described by Rabii[3].

FIGURE 5 *A second order ΔΣ converter.*



5.1 Noise Analysis

Figure 8 shows a simple switched capacitor integrator. We assume that the output is sampled at the end of ϕ_2. The output is contaminated with device noise in three ways:

1. During ϕ_1 the input voltage is sampled on capacitor C_s. If the time available to settle is longer than a few time constants $R_{on1}C_s$ where R_{on1} is on the resistance of the switch, (as it should be for proper operation) the voltage noise sampled on C_s is

†. Actually, since the rise and fall time are finite with duration of 1ns, the comparison happens between the 78th and 79th ns, but it is assumed that the voltage at the input of the comparator does not change significantly within this interval.

FIGURE 6 *The clocks of the circuit of Figure 5.*

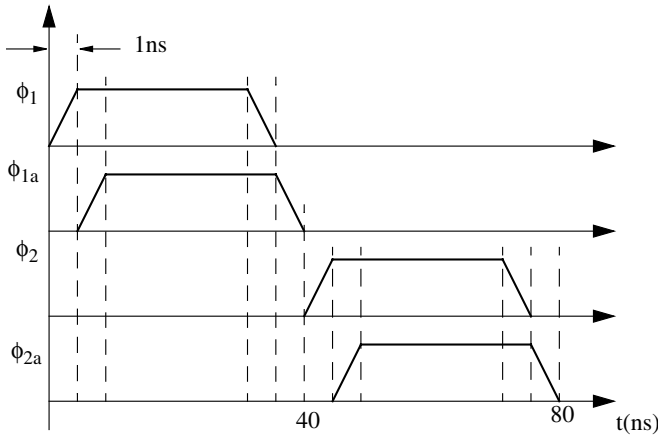


FIGURE 7 *The comparator used in Figure 5.*

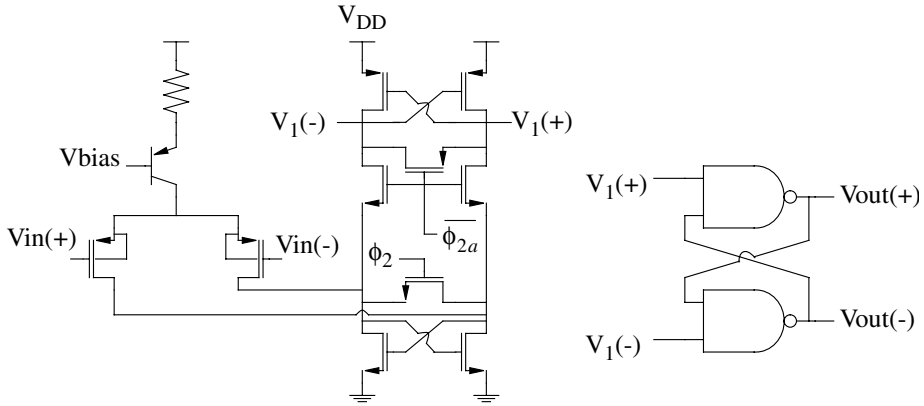
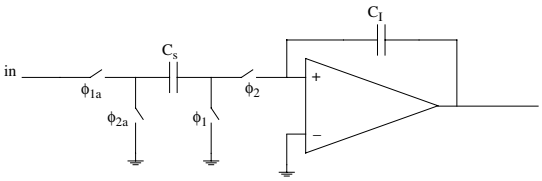


FIGURE 8 *A switched-capacitor integrator.*



white with variance kT/C_s, where k is Boltzman's constant and T is the absolute temperature, independent of R_{on1}. This noise is indistinguishable from the input signal and is transferred to the output during ϕ_2. The PSD of the corresponding output noise is the flat PSD of the input noise multiplied by the magnitude square of the integrator transfer function. Flicker noise of the switches is not an issue because the transistors used as switches operate as resistors in the triode region. Flicker noise manifests itself as small fluctuations in the resistivity, which does not affect the volt-

ages sampled on the capacitors since at the end of every phase there is no current passing through them.

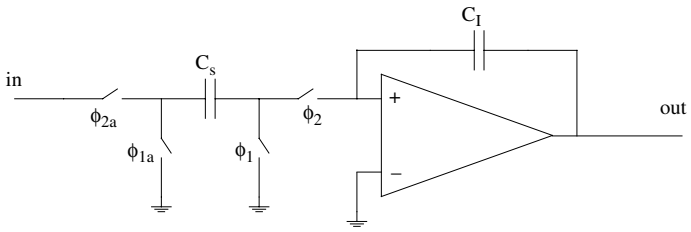
2. During ϕ_2 the circuit generates broadband noise, which when sampled at the output at the end of ϕ_2 is converted to discrete time noise process and its spectrum is folded. The transistors of the opamp as well as the on switches contribute to this noise. If the opamp were ideal with infinite gain at all frequencies the switches would contribute again noise with power kT/C_s on C_s, or $(kT/C_s)(C_s/C_I)^2$ to the output, but in practice this noise contribution is a function of the bandwidth of the opamp and generally depends on the on resistance of the switches R_{on2}. The contribution of the opamp also depends on R_{on2}. In most practical cases however the broadband noise is practically independent of R_{on2} [2].
3. At the end of ϕ_2 some of the broadband noise is stored on C_I, which affects the output in future cycles since this capacitor is never reset. It is equivalent to consider that the charge that corresponds to this noise is stored on C_s during the next ϕ_1 (this happens to be equal to the noise sampled on C_s at the end of ϕ_2). As in Item 1, noise stored on C_s is indistinguishable from the input signal and its PSD is transferred to the output by multiplication with the magnitude square of the integrator transfer function. This noise contribution however is correlated with that of Item 2.

5.2 Cyclostationarity

Here we justify the assumption that the noise generated in every cycle in independent of the processed signal.

Different values of the input signal in different cycles causes different values of the on resistance of the switches. The noise sampled during ϕ_1 is independent of R_{on1} as explained. For the non-subtracting integrator of Figure 8, during ϕ_2 the switches are always at ground potential and have the same R_{on2}. For the subtracting integrator of Figure 9, R_{on2} depends on the input signal and varies from cycle-to-cycle, but the dependence of the generated noise on this resistor is in most cases negligible, as mentioned above.

FIGURE 9 *A subtracting switched capacitor integrator.*



Now consider device noise generated in the opamp. At the end of ϕ_2, the transistors of the opamp operate with the same bias current independent of the output voltage and therefore generate approximately the same noise. At the beginning of ϕ_2, during the transition towards the final output voltage, the opamp possibly slew rates and the bias of the devices and the generated noise is possibly different from cycle to cycle. However, for the proper operation of the switched capacitor filter, the longest time constant of the circuit must be several times smaller than the duration of ϕ_2 and therefore it is reason-

able to consider that the differences in the generated noise in the beginning of the phase have faded at the end when the voltage sampling takes place. Considering flicker noise, the values of the flicker noise sources in the opamp are determined by the long term time average bias and cannot be significantly different form cycle to cycle nor can they be significantly affected by the slew rate time interval.

We justified that the statistics of the generated noise do not significantly vary from cycle to cycle and therefore is cyclostationary. The noise simulations intended to characterize the noise performance of the switched capacitor filter can be performed without input signal.

5.3 Simulation

The reference by Kundert [8] gives some guidelines for the simulation of SC filters and should be read carefully before one attempts to use SpectreRF for this purpose. Switched capacitor circuits are excited by the strong clock waveforms whose rise and fall time are much smaller than the period. SpectreRF is primarily configured for RF circuits in which the strong periodic excitation is usually a smooth function. For this reason, the accuracy parameters of the simulator must usually be tightened in order to obtain a reliable result. It is recommended that in the PNoise analysis a large number of sidebands should be requested to adequately account for noise folding, for example *maxsideband*=20. If there are very small time constants in the circuit compared to the period (e.g. fast sampling circuits), which give rise to wideband noise spectra, the *maxsideband* parameter should be higher so as to include more noise folding.

Simulating an open loop integrator, and even worse a cascade of integrators is vulnerable to convergence problems during the PSS analysis. A slight error in the initial input voltage gets integrated and results in a large difference at the output between the beginning and the end of the period. A small amount of feedback, such as an RC divider with a pole at very low frequencies is often necessary to make convergence possible. In some cases, in order to achieve convergence the introduced pole needs to be at frequencies high enough to affect the transfer function of the system and the output noise spectrum in the band of interest.†

A great improvement in the convergence problems and simulation time can be achieved, if instead of the output noise we seek the input referred noise of the cascade of the two integrators. During the behavioral simulation we can add the corresponding noise signal at the input of the cascade, instead of the output. The input referred noise of the open loop system is equal to that of the close loop system with feedback gain equal to one (or any other noiseless feedback). This is equivalent to just simulating the loop of Figure 1 without the quantizer. The close loop systems have better convergence properties during the PSS analysis and the simulation is generally faster.

†. It was found that PSS convergence is facilitated by performing a PSS analysis with a significant feedback (e.g. small resistor) in the beginning and saving the initial conditions in a file. The PSS analysis is then repeated several times by reducing the feedback and using the initial conditions generated in the previous simulation.

5.4 Closing the Loop

We will now discuss how to close the loop. Directly connecting the output to the input is incorrect, and in fact the input referred noise that simulation provides in this case is different than that of the open loop system. A switched capacitor circuit is a discrete time system, and when closing the loop, during the output evaluation one must feed at the input the output the previous cycle. Some kind of memory is needed to store the output for one cycle, and an ideal S/H can be used for this purpose. Consider the integrator of Figure 8. It is important that to notice that although ignoring the noise, the output voltage stays the same after the end of ϕ_2, until the beginning of ϕ_2 of the next cycle, the output noise must be sampled at the end of ϕ_2 since after that the topology of the circuit changes and the output noise is different. As shown in Figure 10, an ideal S/H can store the output at the end of ϕ_2 and provide it at the input during the next ϕ_1 when it must be read. In a subtracting integrator where the input must be read during ϕ_2, the output of the previous cycle is not available during the whole ϕ_2, because the S/H must obtain the new output at the same time. This problem can be easily solved with a second S/H, sampling the output of the first anytime outside ϕ_2, as shown in Figure 11.

FIGURE 10 *A closed loop switched capacitor integrator.*

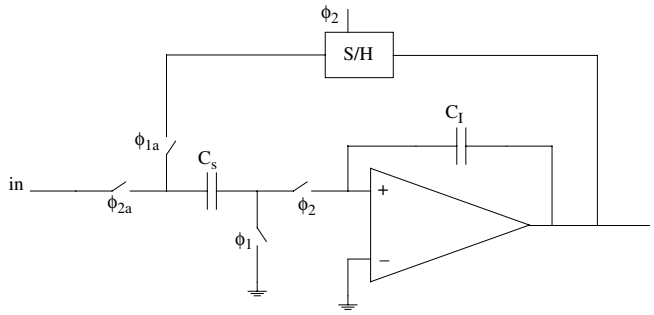
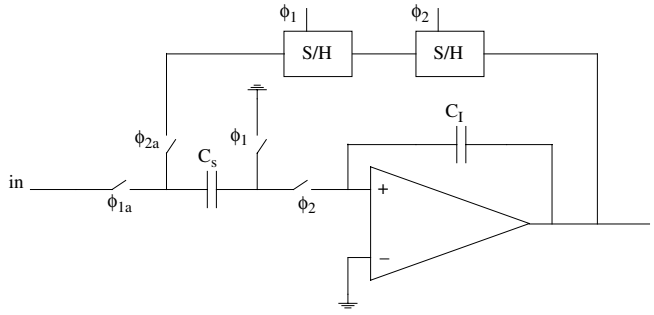


FIGURE 11 *A closed loop switched capacitor integrator where two S/H circuits are needed.*



In a differential structure two S/H circuits can be used, one for each side of the circuit as in Figure 12. In a differential circuit with single ended input such as the first integrator of Figure 5, an ideal S/H can sample the difference of the two output voltages that can then be fed at the input. This is shown in Figure 12, where in order to achieve a unity gain feedback the sampled output voltage is also scaled by 0.5. If necessary, voltage

dependent voltage sources can provide the complement of the output voltage, as shown in Figure 18 on page 16.

FIGURE 12 *A closed loop switched capacitor differential integrator.*

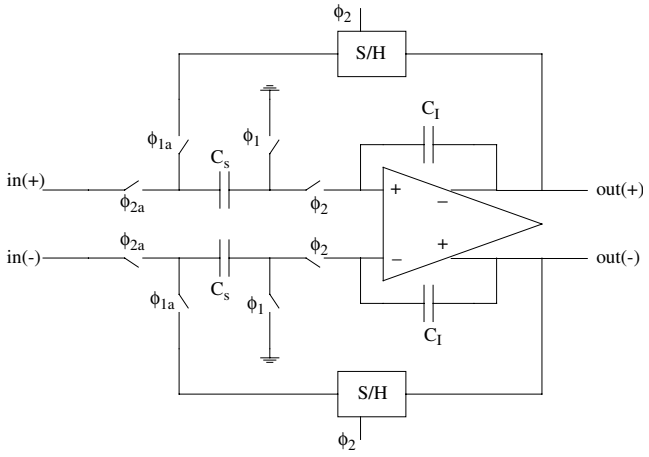
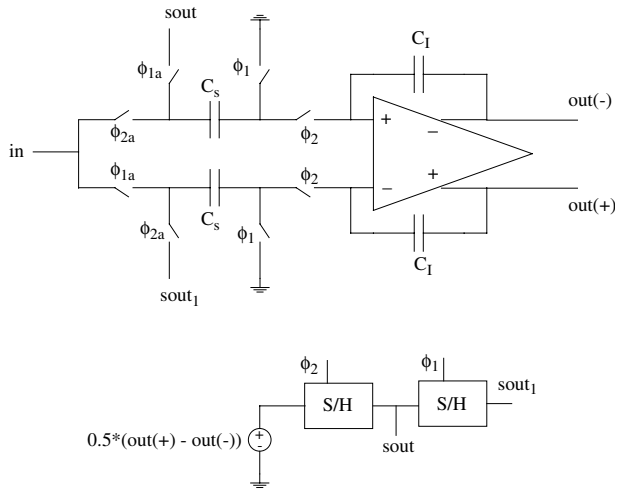


FIGURE 13 *A closed loop single-input, differential-output integrator.*



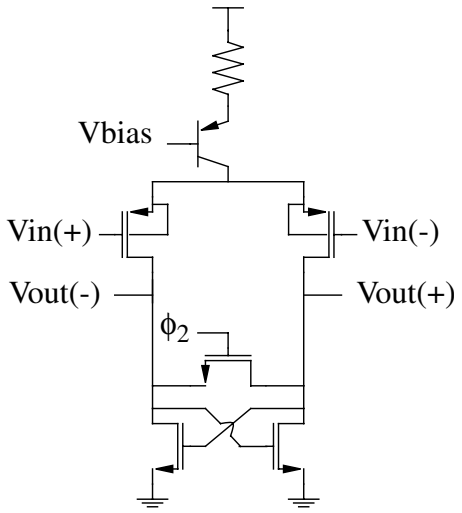
5.5 ADC and DAC Noise

The reference voltage is usually considered noiseless, but if its PSD is known, an appropriate noise signal can be added directly to the input of each integrator during the behavioral simulation. If its continuous time stationary PSD is known, the PSD of the discrete time process can be found by manually folding the spectrum, or directly from SpectreRF by using an ideal S/H circuit as described in Section 4.

As discussed above the effect of the comparator device noise is negligible and the discussion about how to take into account its effect is rather academic. When a strong positive or negative signal is present at the input of the comparator, its device noise does not

affect the comparison. Device noise plays a role only when the input signal is very small. The comparator responds to the sum of the input signal and its input referred noise. The later must be calculated with the comparator in the balanced state, that is with zero input signal, and any systematic offset subtracted. For a continuous time comparator a fixed operating point noise analysis such as this that SPICE or Spectre are capable of performing would provide the PSD of the input referred noise. Since only periodic comparisons as required in ΔΣ converters, the comparators used are usually dynamic with latched output. In continuous time converters, to avoid inaccuracies resulting from uncertainties in the response delay when the input is small, the latch is usually clocked a certain amount of time after the evaluation phase has started. A typical comparator is shown in Figure 7. It resets during ϕ_2 and makes a comparison at the end of this phase. The duration of ϕ_2 is large enough for the circuit to go in steady state in the configuration of Figure 14. Then a fixed point noise analysis with the circuit permanently in the state of ϕ_2 can be used to find the spectrum of the broadband input referred noise (assuming that the output is taken as the voltage across the transistor controlled by ϕ_2, or the current difference between the two branches), which can then be folded to provide the PSD of the discrete time input referred noise. Alternatively SpectreRF with an ideal S/H at the output and another one before the input can be used to take into account the aliasing effects in the input referred noise. If SpectreRF is used, we can as well use the real clock waveforms and sample the output at the end of ϕ_2 and the input anytime outside ϕ_2 instead of simulating the circuit permanently in the state of Figure 14.

FIGURE 14 *The comparator of Figure 7 in the reset phase.*

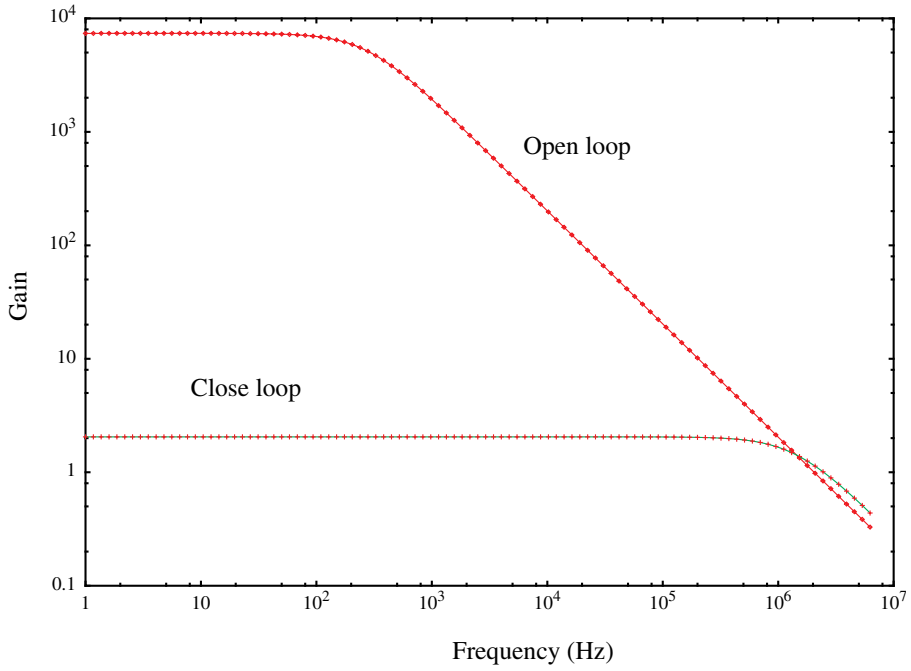


5.6 Results

We present first some simulation results for the differential integrator of Figure 12. The gain of the open and close loop systems are shown in Figure 15. The output noise is shown in Figure 16 (not being compensated for $\sin(x)/x$) and the input referred noise is shown in Figure 17. These results are shown up the frequency $f_s/2$ = 62.5 KHz. Qualitatively the shape of the input referred noise is explained as follows. Low frequencies are

dominated by the flicker noise, at higher frequencies the noise is flat representing broadband input noise, and at frequencies close to $f_s/2$ the input referred noise increases because the output broadband noise is divided by the small integrator gain.

FIGURE 15 *Simulated gain from the integrator of Figure 12, or the second integrator of Figure 5.*



The input referred noise of the circuit of Figure 5 from the equivalent linearized closed loop circuit of Figure 18 is shown in Figure 19. The input referred noise of the first integrator alone is also shown (during this simulation loading of the output with the 2nd integrator was not included). At low frequencies where the gain of the first integrator is very high the input referred noise of the cascade is determined completely by the first integrator. At higher frequencies however, the second integrator contributes significant noise. Because of the logarithmic frequency scale in this graph, this noise represents significant out-of-band noise power.

A discrete time transfer function with 7 poles and 7 zeros was fit to the input referred noise of Figure 5 and the result is shown in Figure 20.† The available fitting routine worked in continuous time and the bilinear transformation was used to transform the simulation output from discrete time to continuous time (stretch the frequency interval from $[0, f_s/2]$ to $[0, \infty]$) and then to transform the obtained transfer function from the s-domain to the z-domain. When the bilinear transformation is used for this purpose the obtained discrete time transfer function has equal number of poles and zeros. In fact any transfer function can be represented with equal number of poles and zeros, since it can be flat at very high and very low frequencies that are not of interest. Such a transfer function can be written in pole residue representation as

†. Carlos Cohelo provided the fitting routine.

FIGURE 16 *Simulated output noise from the integrator of Figure 12.*

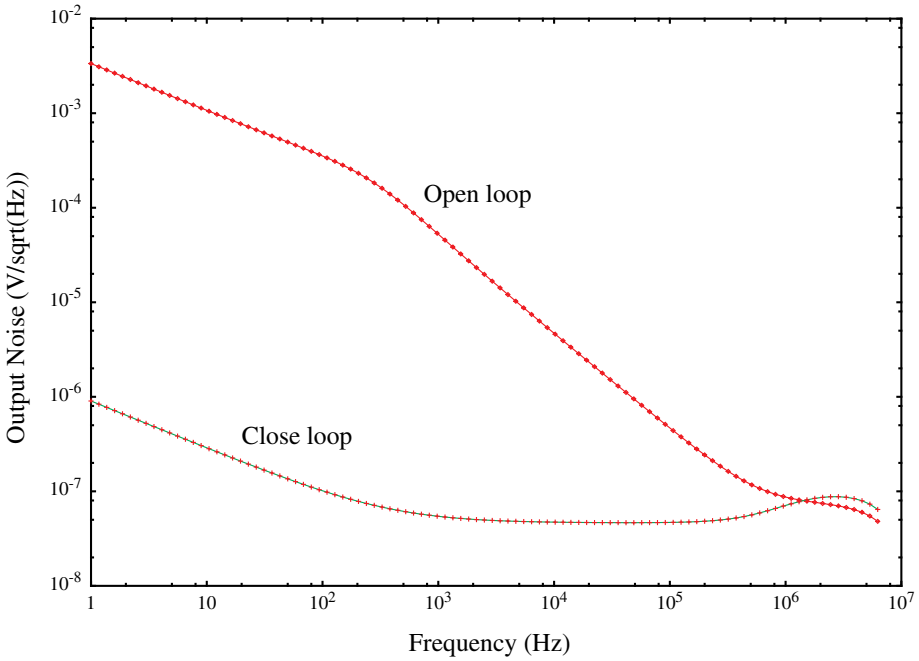


FIGURE 17 *Simulated input referred noise from the integrator of Figure 12.*

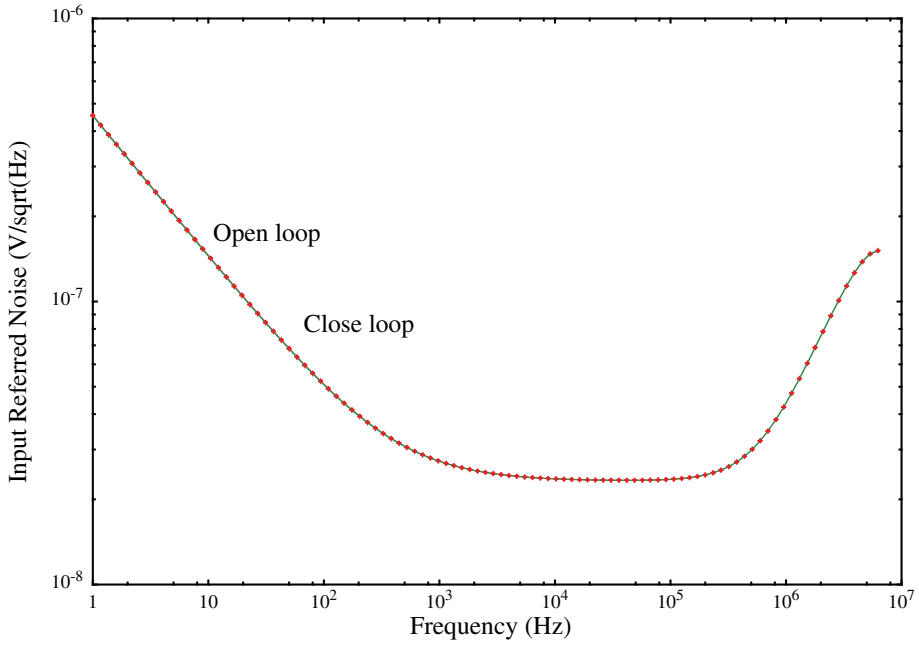


FIGURE 18 *Close loop linearized circuit for the converter of Figure 5.*

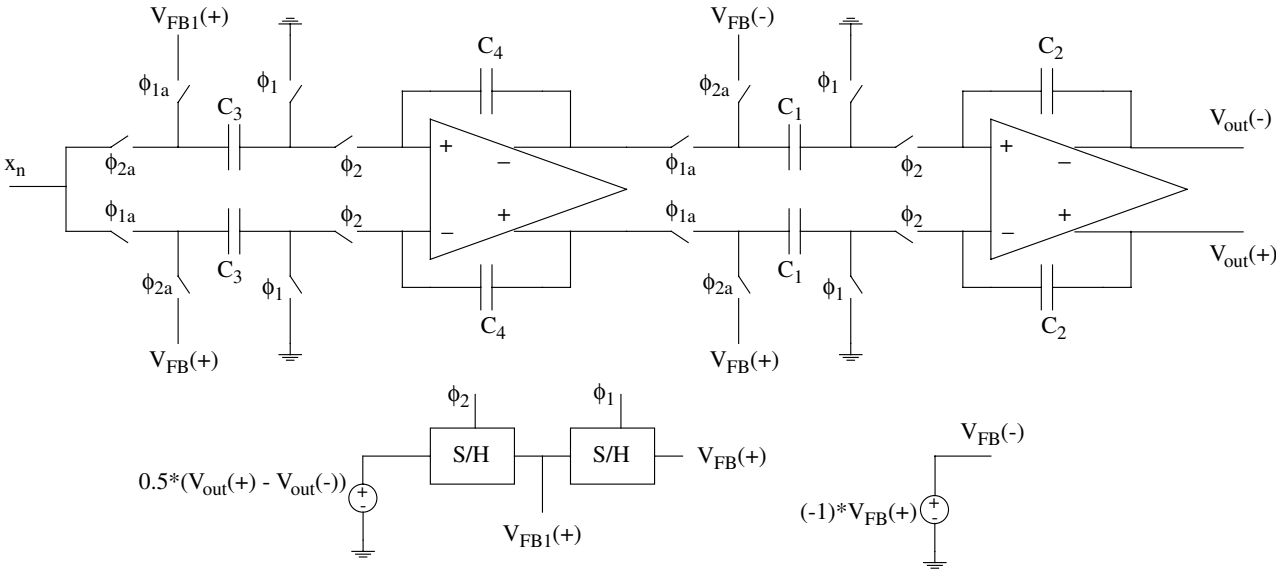
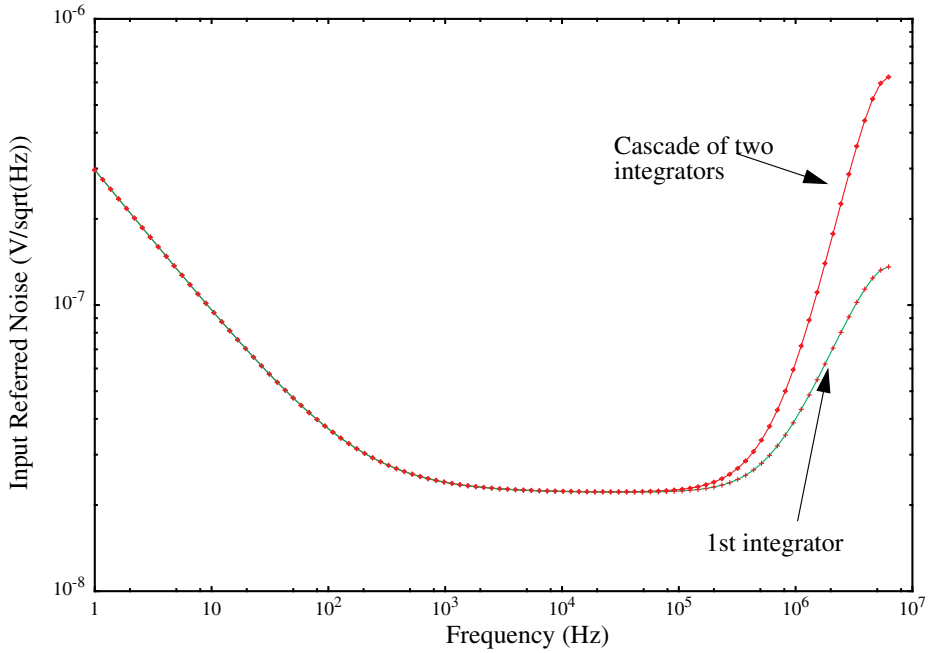


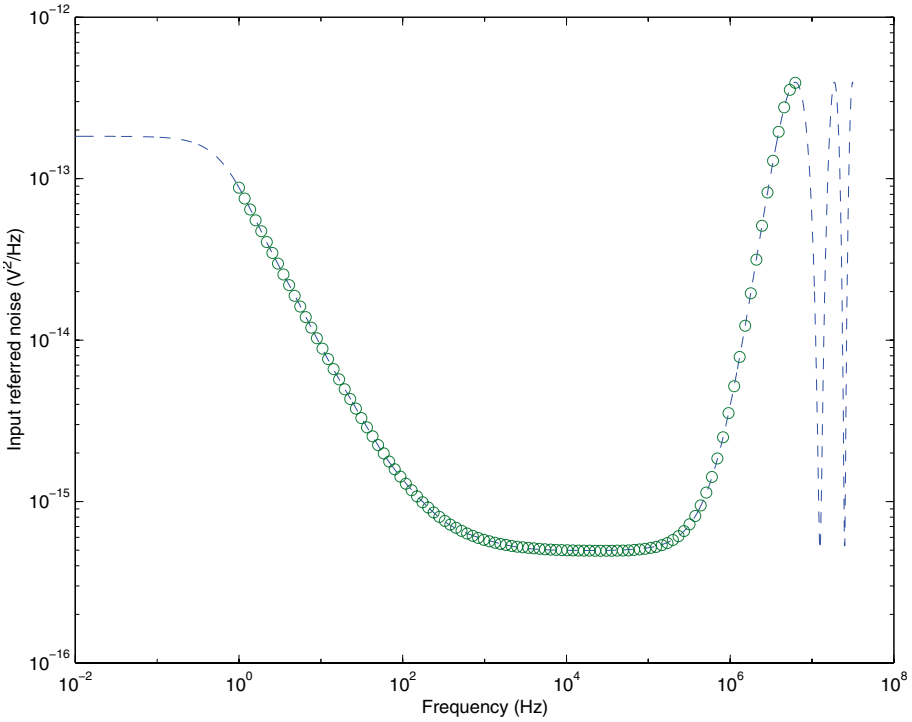
FIGURE 19 *Input referred noise of the loop of Figure 18.*



$$H(z) = c\left(1 + \frac{r_1}{z - p_1} + \ldots + \frac{r_n}{z - p_n}\right), \tag{8}$$

which leads to the following discrete time filter implementation.†

FIGURE 20 *Fit of a discrete time transfer function to the numerical data obtained from SpectreRF (○).*



$$y(k) = c\sum_{i=1}^{n} x_i(k)r_i + w(k), \tag{9}$$

$$x_i(k+1) = p_i x_i(k) + w(k) \qquad i = 1, \ldots, n \ , \tag{10}$$

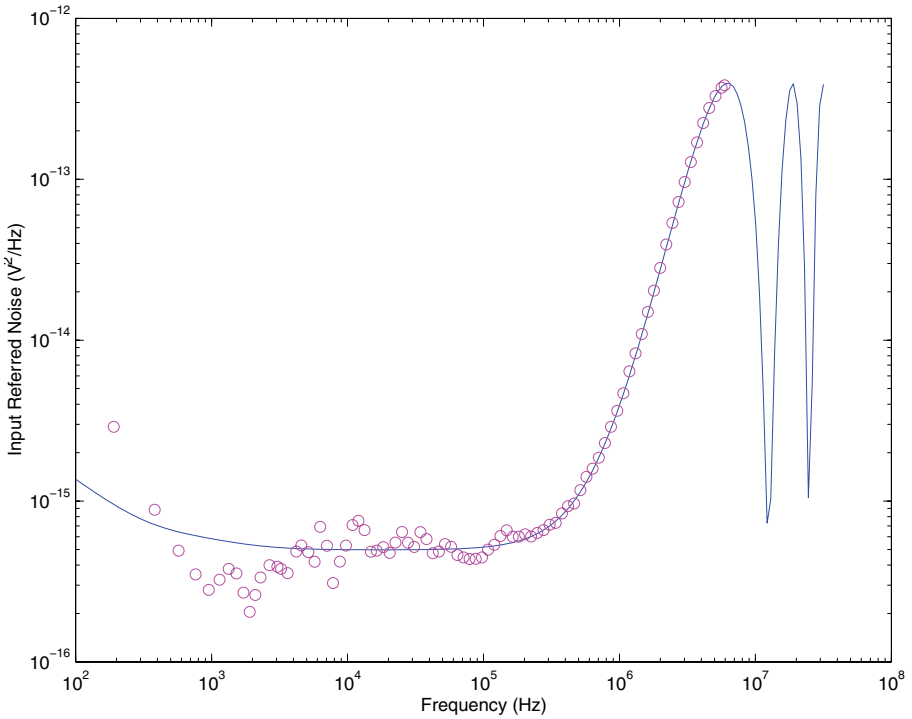
where $y(k)$ is the filter output, $w(k)$ is a white noise input, and $x_i(k)$ are the n states. The above realization requires the same number of multiplications and additions as the straightforward recursive realization and in addition involves independent state equations and is stable even when there are poles at very low frequencies (very close to 1), while the recursive realization might have problems. These very low frequency poles are present in our application because they represent flicker noise.

The obtained discrete time filter was fed with white noise and the output was processed with a PSD estimator. The result is shown in Figure 21 together with the target PSD. Very good agreement is observed at high frequencies, while at low frequencies the estimation is impaired by the finite observation time.

The second order converter of Figure 5 was implemented in difference equation form in Verilog-A and simulated with SpectreRF. A digital filter was also included in the Verilog-A file and noise with PSD equal to the input referred noise was injected at the input together with a sinusoid of frequency f_{sig} = 3.051757 KHz = f_s/4096 and amplitude

†. The pole-residue filter realization is Joel Phillips' suggestion.

FIGURE 21 *The output of the noise generating filter was processed by a PSD estimator and is shown together with the target PSD.*

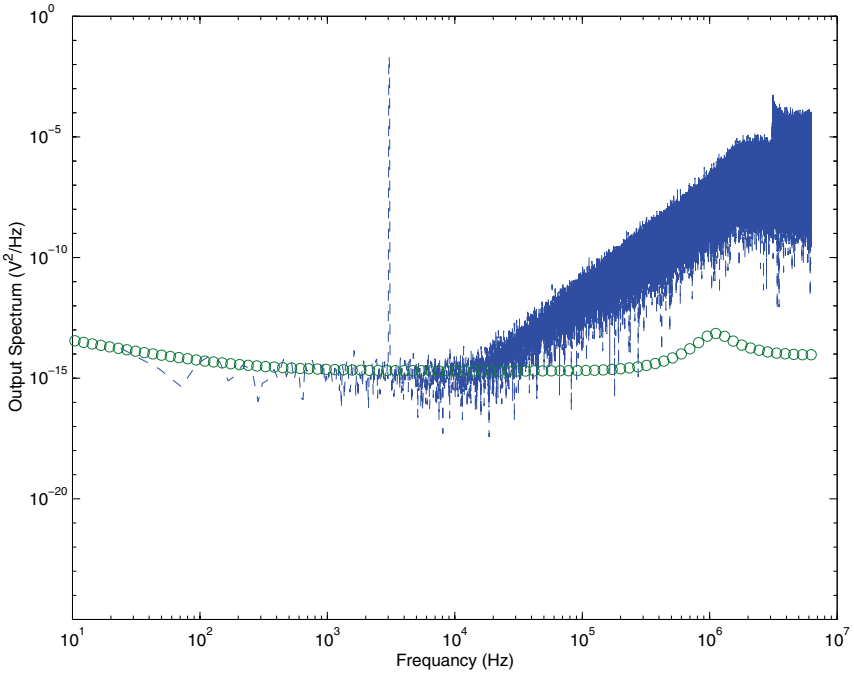


0.65 V. The output spectrum is shown in Figure 22. The device noise generating filter was turned off and the result is shown in Figure 23. The spectrum was calculated with a PSD estimator using a Hanning window of length equal to the number of data points.†

To examine the combined effect of the quantization and device noise in frequency bands where the one of the two kinds is dominant or they have approximately equal contribution, the output was considered to pass from a brick wall filter with cut-off frequency varying from about 4 KHz to 100 KHz. The SNR was calculated considering quantization noise only, device noise only, and their combined effect. The result is shown in Figure 24. In the area that the quantization noise is dominant the device noise does not seem to have a significant dithering effect.

†. This is equivalent to applying a normalized Hanning window to the data and then performing an FFT. It is worth noting that FFT on the raw output data (which is equivalent to applying a rectangular window), gave similar results with the above method when only quantization or only device noise was present, but a low frequency noise floor well above the expected output device noise, when both quantization and device noise were present. I have not explained that yet. It is possible that it is related with the fact that the rectangular window has a high frequency components and allows higher leakage from high to low frequencies than the Hanning window.

FIGURE 22 *The output spectrum of the converter of Figure 5, when device noise effects are included in the behavioral simulation. The device noise at the output of the feedback loop is also shown (○).*



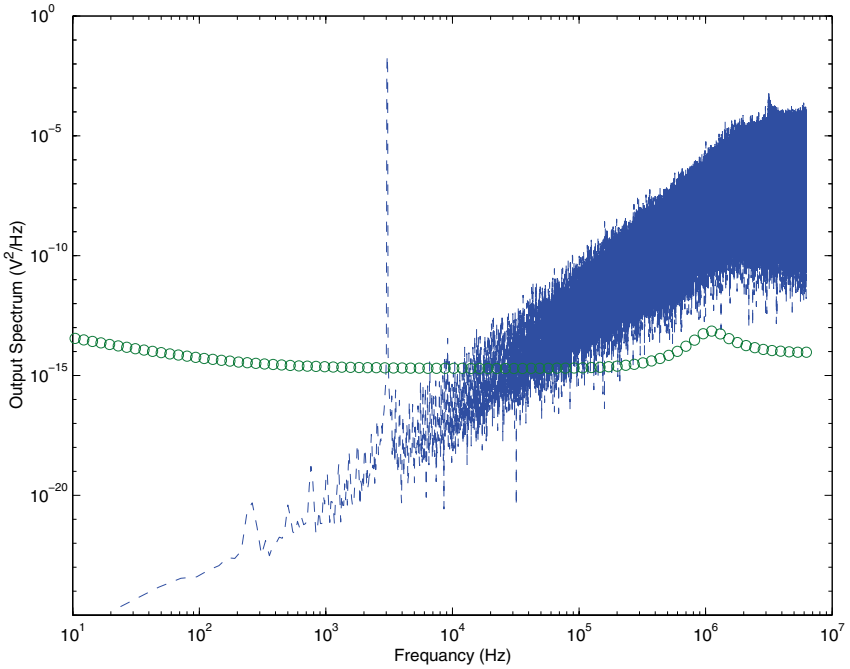
6 Conclusions

A methodology was described with which the device noise effects can be included in the behavioral simulation of ΔΣ converters. It was justified that by discarding some redundancy, a discrete time noise process is sufficient to describe the device noise effects of the analog circuitry in the behavioral simulation. We examined in detail how the PSD of such a discrete time noise process can be obtained from circuit level simulation with SpectreRF. A discussion was included about how to obtain the desirable noise statistics from the close loop filter instead of the open loop because it is easier to simulate. Sample results from a second order ΔΣ converter were shown. In this particular example we found that the quantization noise is not significantly affected by the device noise and one could obtain the same results by adding the quantization and device noise calculated separately. However it is possible that in some cases the device noise will have a considerable effect on the quantization noise.

6.1 If You Have Questions

If you have questions about what you have just read, feel free to post them on the *Forum* section of *The Designer's Guide Community* website. Do so by going to *www.designers-guide.org/Forum*.

FIGURE 23 *The output spectrum of the converter of Figure 5, without device noise effects. The device noise at the output of the feedback loop is shown (○).*



Acknowledgments

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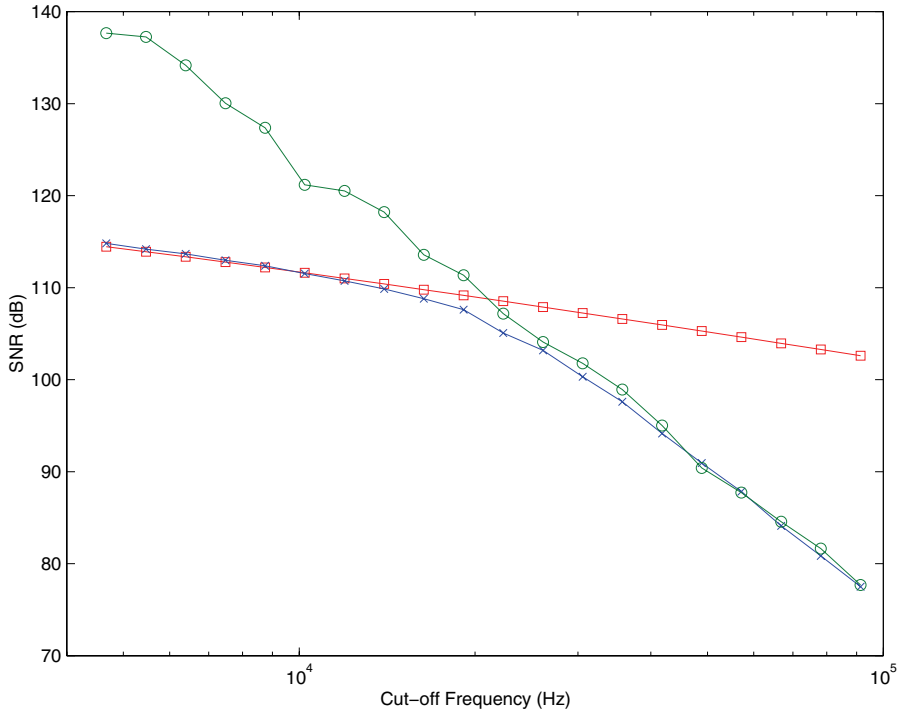
FIGURE 24 *Output SNR of the converter of Figure 5, taking into account only quantization noise (○), only device noise (□), and the combined effect of both, taking into account their interaction (×).*



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