Comparator Metastability Analysis

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This paper describes a simple method for predicting the metastability error rate for a latching voltage comparator when used in an A/D. It first derives the formula used to predict metastability and then describes a simple simulation method to compute the error rate.

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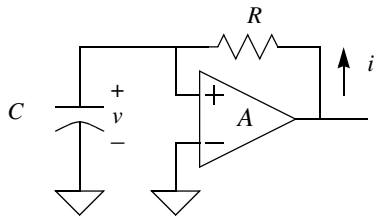
1 Metastability

Metastability is a problem that occurs in all latching comparators when the input is near the comparator decision point [3]. The problem occurs when the comparator takes more time to switch to a valid output state than is available in the sample interval. In order to calculate the probability of this happening, a simple model of the comparator latching process is first described. Figure 1 shows the simple circuit used to model the latch during the latching process.

FIGURE 1 *A simple circuit models a latching comparator during the latching process.*



This model is used to develop a formula that gives the output voltage at the time it will be sampled versus the input voltage. In this circuit

$$i = \frac{Av - v}{R} \tag{1}$$

where A is the gain of the amplifier. Then

$$\frac{dv}{dt} = \frac{i}{C} = \frac{(A-1)v}{RC}, \tag{2}$$

$$\frac{1}{v}\frac{dv}{dt} = \frac{A-1}{RC}. \tag{3}$$

Integration both sides of (3) yields

$$\ln(v) = \frac{(A-1)}{RC}t + K \tag{4}$$

where K is the integration constant. Exponentiating both sides of the equation leads to

$$v = K_2 e^{\frac{(A-1)t}{RC}} \tag{5}$$

where K_2 is a constant (equal to e^K). To solve for K_2, assume at $t = 0$ the output voltage of the comparator is v_o. Solving for K_2 then yields

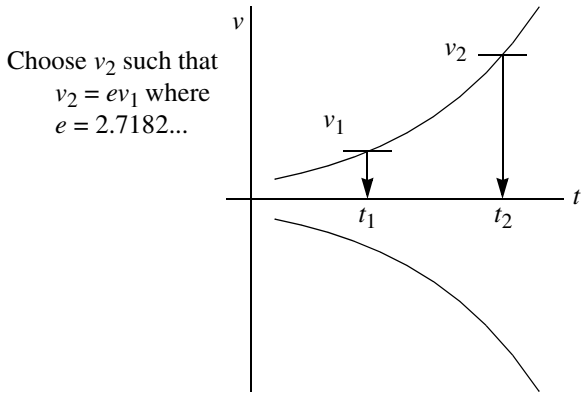
$$K_2 = v_o. \tag{6}$$

The voltage at the latch can therefore be written as

$$v = v_o e^{\frac{(A-1)t}{RC}}. \tag{7}$$

This describes the behavior of the latching comparator as it latches. Of course, the comparator output values will eventually limit at the full voltage swing of the comparator. We next need to find a way to measure the RC of the comparator. This can be done with simulation by placing near zero volts across the comparator input and then switching the comparator to the latch state. The output of the comparator will switch in a high or a low direction as shown in Figure 2.

FIGURE 2 *The output voltage of the latch of Figure 1 as it changes state.*



Pick an arbitrary voltage v_1 at t_1 and then measure the time it takes for the voltage to reach the voltage v_2 where $v_2 = ev_1$ with both measured with respect to the 0 crossover state (common mode of comparator output). Now

$$e = \frac{v_2}{v_1} = \frac{e^{\frac{(A-1)t_2}{RC}}}{e^{\frac{(A-1)t_1}{RC}}} = e^{\frac{(A-1)}{RC}(t_2 - t_1)}. \tag{8}$$

Taking the natural log of both sides gives

$$1 = \frac{A-1}{RC}(t_2 - t_1). \tag{9}$$

Solving for RC yields:

$$RC = (A-1)(t_2 - t_1) \tag{10}$$

Substituting RC into (7) gives

$$v = V_o e^{\frac{t}{t_2 - t_1}} \tag{11}$$

where V_o is the initial starting state for regeneration.

One runs into a metastability problem when the output of the comparator does not reach a valid logic level in the specified time interval. In cases where a slave latch follows the comparator, the logic level out of the slave latch must be correct within the required time period. If the logic following the slave latch requires less than half a clock cycle, then

the regeneration time of the second latch must be analyzed as well. In any event, the following derivation will assume that the comparator output must switch to V_L by time *T*.

Let ε be the smallest starting regeneration value that will not cause an error by time *T*. Then

$$V_L = \varepsilon e^{\frac{T}{t_2 - t_1}} \tag{12}$$

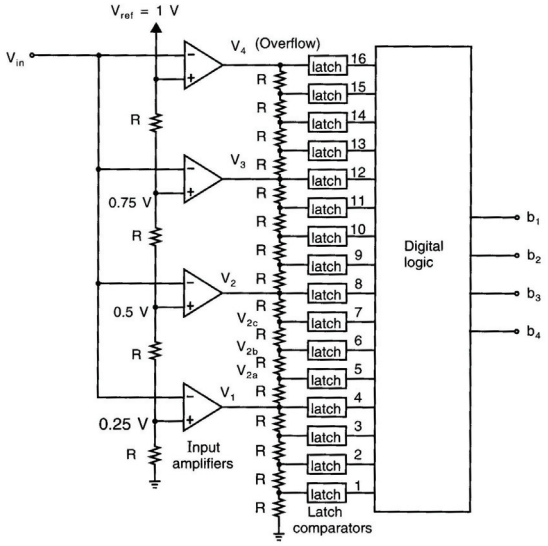
where $t_2 - t_1$ is the time difference measured earlier. Solving for ε yields

$$\varepsilon = V_L e^{\frac{-T}{t_2 - t_1}} \tag{13}$$

The probability that the latch of the comparator is starting out with ε or lower across it is equal to the probability of a metastable error.

Assume that the comparator is used in a interpolating flash converter, as shown in Figure 3. In this case, there is an amplifier between the input of the converter and the input to the comparator. Call the gain of this amplifier A_{UL}. If there is no amplifier, then set $A_{UL} = 1$.

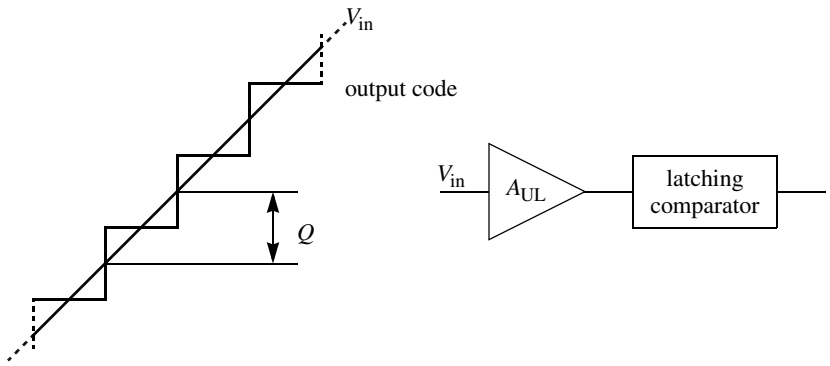
FIGURE 3 *An interpolating flash converter.*



Define *Q* to be the quanta size at the input to the converter, as illustrated in Figure 4. So *Q* is the maximum amount of change in the voltage at the input that can be made without causing a transition in the output of an ADC. Including the effect of an input amplifier, the size of quanta at the latch input is QA_{UL}.

Next, assume that the probability of an input is a uniform distribution across a code of the A/D. This assumption is valid if there is noise or signal at the A/D input toggling several codes.

FIGURE 4 *The quanta size at the input of the ADC is Q. The quanta size at the input of the comparator is QA_{UL} where $A_{UL} = 1$ if there is no amplifier before the comparator.*



The range of latch voltages that cause trouble (metastability errors) at $t = 0$ is from $-\varepsilon$ to $+\varepsilon$. The probability of this happening is therefore

$$P_{error} = 2\varepsilon/(A_{UL}Q). \tag{14}$$

Combining (13) and (14) yields the probability of a metastability error

$$P_{error} = \frac{2V_L}{A_{UL}Q} e^{\frac{-T}{t_2 - t_1}}. \tag{15}$$

where Q is the quantum size at comparator input in volts,

V_L is the minimum valid logic level comparator must generate,

A_{UL} is the comparator unlatched gain,

T is the maximum time period allowed for the comparator to make correct decision, and

$t_2 - t_1$ is the time difference measured in simulation as described earlier.

An example is now given to illustrate this method.

First, in a simulation of a comparator 10 uV is placed across the input and the comparator is switched to latch. The output of the comparator is an exponentially increasing voltage as shown in Figure 2. Next find where the voltage has changed 10 mV and call this time t_1. Now find when the voltage has change 27.18mV from its starting position. This time is t_2. With $t_2 - t_1$ known, (let us assume 65ps), next calculate the size of a quantum at the comparator input. In this example, let us assume that the A/D input has a quantum size of 16mV and an autozero stage with a gain of 2.5. The size of a quantum at the comparator input is therefore 40mV (Q) in this case. Next, assume the voltage gain of the comparator in the unlatch state is 4 (A_{UL}). Finally, one must find the V_L which is the output level which the comparator must reach in order for the A/D not to make a mistake in the time interval. Let us assume that the first latch is followed by a second latch (slave) which is switched to the unlatch state when the first stage is latched. During this time the second stage acts as an amplifier. Let us assume that the gain of this second stage is 4. If the output of the second stage must reach 200 mV, the output of the first stage latch must reach 50 mV.

If the A/D must run at 320 MHz and the logic following the comparators requires 1/2 a clock cycle, the time T can be calculated to be $1/(2 \times 320 \times 10^6) = 1.56$ ns. Now we have all the values for the (15).

Therefore

$$P_{\text{error}} = \frac{2 \times 0.05}{4 \times 0.04} e^{\frac{-1.56\times10^{-9}}{65\times10^{-12}}} = 2.36\times10^{-11} \text{ errors/sample}. \quad (16)$$

If two latching stages are in series forming a master slave structure, the metastability equation becomes

$$P_{\text{error}} = \frac{2V_{\text{L}}}{A_{\text{UL}_1} A_{\text{UL}_2} Q} e^{\frac{-T_1}{t_2 - t_1}} e^{\frac{-T_2}{t_2 - t_1}} \quad (17)$$

where A_{UL_1} is the master comparator unlatched gain,

A_{UL_2} is the slave comparator unlatched gain,

T_1 is the time interval available for the master comparator, and

T_2 is the time interval available for the slave comparator.

1.1 If You Have Questions

If you have questions about what you have just read, feel free to post them on the *Forum* section of *The Designer's Guide* website. Do so by going to *www.designers-guide.org/Forum*.

Other Reading

[1] Harry J.M. Veendrick. The behavior of flip-flops used as synchronizers and prediction of their failure rate. *IEEE Journal of Solid-State Circuits*, April 1980, pp.169.

[2] Rudy van de Plassche. *Integrated Analog-to-Digital and Digital-to Analog Converters.* Kluwer Academic Publishers, 2003.

[3] Clemenz L. Portmann and Teresa H. Y. Meng. Metastability in CMOS library elements in reduced supply and technology scaled applications. *IEEE Journal of Solid-State Circuits*, January 1995, vol. 30, no. 1, pp. 39-46.