A Substrate Modeling Methodology

Glenn Murata
Amalfi Semiconductor

Ken Kundert
Designer's Guide Consulting, Inc.

Version 1, 1 January 2006

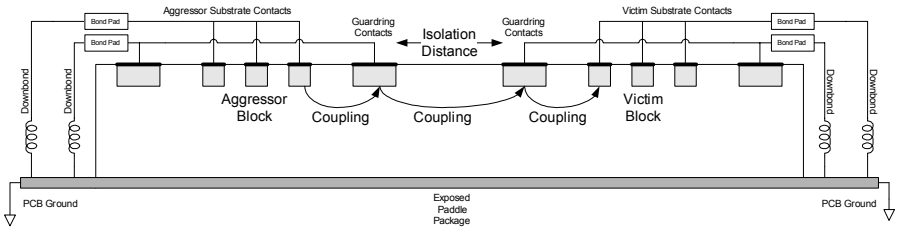
This document describes a methodology for estimating the coupling of signals through the substrate of a mixed-signal integrated circuit.

Last updated on May 11, 2006. This paper was originally written in June 2005 and published in January 2006. You can find the most recent version at www.designers-guide.org. Contact the author via e-mail at gmurata@amalfisemi.com.

1 Introduction

The idea in this methodology is to develop a set of simplified models and simplifying assumptions that allows one to roughly predict the degree of coupling through the substrate between an aggressor block and a victim block. The goal is to assess the need for, and the effectiveness of, various mitigation strategies such as adding guard rings. To do so, we will start with the basic physical description of the situation shown in Figure 1.

FIGURE 1 *Cross section of a chip with an aggressor block, two guard rings, and a victim block.*



Here we assume a relatively high resistivity substrate (~10 Ω-cm) and closely spaced structures as compared with the substrate thickness, which allows us to ignore deep coupling. As such, there is no direct coupling between the aggressor and the victim. Instead, the aggressor affects the first guard ring, which affects the second, which then affects the victim. In this way the problem can be broken into 5 pieces:

1. Given the input signals, how much signal is injected into the substrate by the aggressor block?
2. Given the signal injected into the substrate by the aggressor, how much signal is injected onto the first guard ring?
3. Given the signal injected onto the first guard ring, how much signal is injected onto the second?
4. Given the signal injected onto the second guard ring, how much signal is injected onto the substrate contacts in the victim block?
5. And given the signal injected onto the substrate contact in the victim block, how does this affect the output of the system?

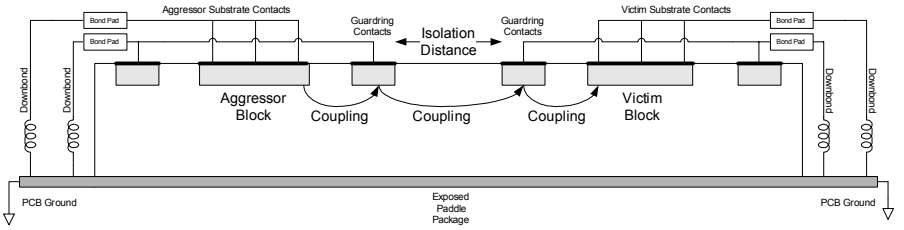
These assumptions allow us to simplify the analysis by decomposing it into several steps. However there is more that can be done.

2 Aggregate Model of the Blocks

Within the blocks, it is considered a good design practice to place substrate contacts immediately adjacent to transistors. This helps reduce coupling and prevents latch up. These substrate contacts are then connected together through metal bias lines. This practice has the effect of making all the transistor substrate regions be at the same voltage. These metal bias lines allow us to approximate the many contacts as one large substrate region, as shown in Figure 2.

In many processes the design rules allow substrate contacts to be less than 1μm apart, so in comparison giving 50μm or 100μm of space seems large. However, if the substrate is

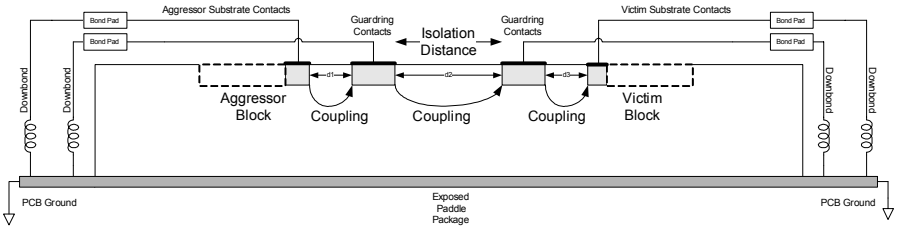
FIGURE 2 *A simplified model of the substrate regions in the aggressor and the victim.*



300µm deep then this 50µm of space between contacts or guard rings is not large. In this case there are significant coupling fields and current flow at the surface of the die. Current tends to flow even more at the surface of the substrate for higher frequencies as well. To further support current flow at the surface we note that many processes place a global p-well layer across the die that can have a conductivity that is 100× more conductive. The presence of this p-well is a well known isolation problem and guard rings are only one technique used to break-up the p-well region.

If guard rings are closely spaced, relative to the substrate depth and adjacent to other blocks on all sides, then the substrate region close to one side of the guard ring dominates the coupling, so the model can be further simplified by only including the substrate region of the blocks that are close to the guard rings, as shown in Figure 3.

FIGURE 3 *A further simplified model of the substrate regions in the aggressor and the victim.*



3 Specifying Isolation Performance

If we can simplify the scope of our analysis down to regions in the silicon that can be readily identified and if these regions can be readily modeled then we can specify the needed isolation performance of the region modeled for the given input and the maximum allowable output.

Given the simplified analysis scope and the insight noted in the introduction about the regions that need to be modeled, we find the following questions lead us to the isolation specification.

1. At what signal level (in dBV) does substrate noise under the victim exceed the maximum allowable output level of the block? In the case of an LNA then at what substrate signal level does the substrate output signal exceed the LNA output noise.
2. What is the substrate signal level of the aggressor given a worse case input signal? In the case of a digital block we need to determine signal levels (in dBV) of the frequency spurs expected from the block.

3. Now we know how much isolation (in dB) we need in order to keep the substrate noise contribution below the maximum allowable output level of the victim block.

Isolation (in dB) = Aggressor substrate signal level (in dBV) – Victim substrate sensitivity level (in dBV)

It is well understood that isolation is needed between known aggressors and known victims but most do not know how much isolation is needed and how to characterize how much isolation is achieved with the layout and circuit structures they have employed. Many best practices have been developed but it has been difficult until recently to determine which ones provide the most benefit and in some cases which actually worsen our isolation under certain conditions. Given this analysis methodology we can now determine if we can design better methods to achieve the calculated isolation specifications.

The following sections discuss a way of answering these questions through simulation and suggest some new steps in the block development flow that will help the chip designer with assuring the chip integrated integrity.

Before we move on it is worth observing that given our past uncertainty in our isolation performance, we have clearly learned that our first line of defense is to handle frequency planning such that unwanted signals don't fall in our frequency bands of interest. It is better not to have a noise issue in the first place. It is worth re-emphasizing that with analysis or not our first line of defense is a good frequency plan. Only if we have no way of moving the corrupting signal do we depend on on-chip techniques and ultimately separating circuits on to different die. Also, analysis in many cases will tell us what we already know in that the isolation specification is difficult or impossible and our known isolation techniques are limited.

4 Modeling the Substrate

Now, three models can be developed of the substrate: the model from the aggressor substrate to the first guard ring, the model between the two guard rings, and the model from the second guard ring to the victim substrate. The goal is to be able to use this information to design a substrate coupling mitigation strategy, and so a variety of sizes and spacings should be modeled. Since each segment is modeled independently, the models can be mixed and matched to try various physical layouts. There are several papers that propose resistive substrate models and extraction methods [1]. The actual model can be extracted either from measurements from a series of test chips, or by using an electromagnetic system simulator. Sonnet Software provides Sonnet Lite [2], a free reduced capability simulator that can be used successfully in this situation. The model should be in one of the forms shown in Figure 4. Simulation results from Sonnet Lite and other papers [3] show that the assumption of a purely resistive substrate model is a good approximation up to about 10GHz. Above 10GHz substrate capacitance needs to be taken in to account.

These models are then combined, along with the inductance between the guard rings and ground. Typically down bonding from the pads to the package paddle is used, which shortens the path to ground relative to going through one of the package pins. This results in lower inductance, typically around 0.6 nH. Now the structure of Figure 3 is modeled as shown in Figure 5.

FIGURE 4 *Simple coupling models for a substrate components.*

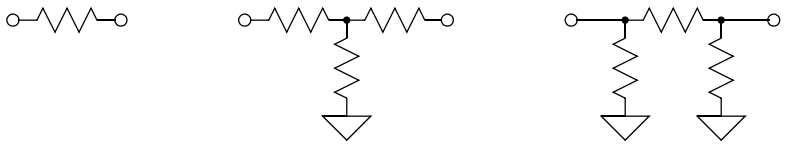
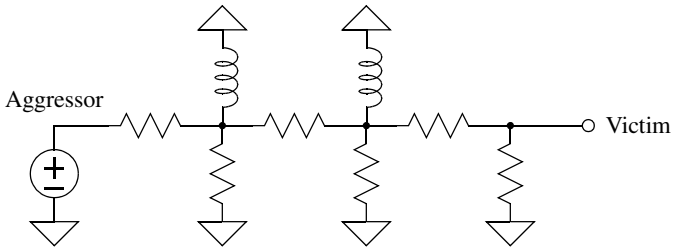


FIGURE 5 *A model of the substrate shown in Figure 3.*



It is important to note that the inclusion of the inductors gives this network a frequency dependence that plays a factor at RF frequencies. A typical frequency response plot is shown in Figure 6 as an example.

This rough analysis gives us an order of magnitude estimate of achievable isolation and insight to the frequency dependence of our isolation structures.

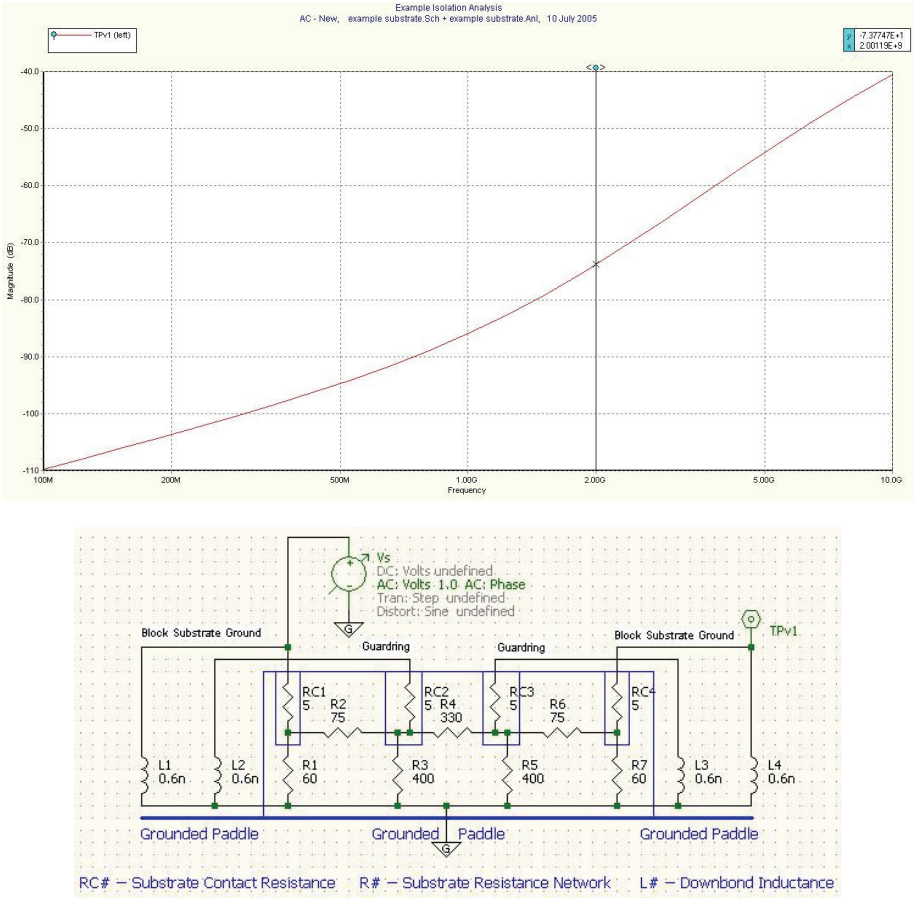
Though we have made the simplifying assumption that the majority of the fields and currents are near the surface of the substrate we know that there are fields and currents that extend into the substrate. Our values for the substrate model resistance will vary due to these unaccounted for currents. Once real floor-plan layouts are made with guard rings then a final verification of the simplified analysis should be checked with a commercially available substrate analysis tool or electromagnetic simulator (EM simulator).

5 Modeling the Aggressor

The aggressor is usually a large block of digital circuitry. It can be simulated with either a circuit simulator such as Spectre or a timing simulator such as UltraSim. It is critically important to model the substrate network well. In particular, the inductance between the substrate network and ground should be included in the simulation. Then the block should be simulated with a representative set of input data vectors and the signal on the substrate lines observed. In particular, the power spectral density of the signal should be recorded.

If modeling the aggressor is too much trouble, one can often just make the assumption that there is around 10-30 mV on the aggressor's substrate lines.

FIGURE 6 *Example isolation analysis results and schematic.*



6 Modeling the Victim

Once the aggressor and substrate have been modeled, the models can be combined to determine the signal level on the substrate at the victim. Then it is a matter of computing the affect of this signal on the output of the circuit. This involves a circuit simulation. If the victim is a simple linear circuit, such as an amplifier, a Spectre's AC or XF analysis is sufficient. If it is a periodically operating circuit, or one that can be modeled as a periodically operating circuit, SpectreRF's PAC or PXF can be used. Otherwise, a full transient analysis would be necessary.

It is interesting to note that the signal levels in the coupling analysis are intentionally small so they lend themselves to linear small signal analysis. Small signal analysis will give us our frequency response from substrate to output very quickly and efficiently. We then determine our sensitivity to substrate noise levels by sweeping the noise power level in the AC analysis to determine when our output signal begins to be dominated by substrate noise as opposed to signal path generated block noise.

7 Conclusion

This methodology for predicting substrate coupling is both simple and effective. It can be used both in the floor-planning phase and the verification phase. Once you have used this methodology several times, you can generally build up models, experience, and rules of thumb that will allow you to avoid substrate coupling issues with little difficulty.

7.1 If You Have Questions

If you have questions about what you have just read, feel free to post them on the *Forum* section of *The Designer's Guide Community* website. Do so by going to *www.designers-guide.org/Forum*.

References

[1] A. Samavedam, A. Sadate, K. Mayaram, T. Fiez, A scalable substrate noise coupling model for design of mixed-signal IC's. *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 895-904, June 2000.

[2] *Sonnet Lite*. Sonnet Software, Inc. *www.sonnetsoftware.com*.

[3] R. Singh, A review of substrate coupling issues and modeling strategies. *IEEE 1998 Custom Integrated Circuits Conference*, pp. 491, May 1998.