SILICON BJT MODELING USING VBIC MODEL

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In the paper, we develop an accurate and efficient methodology to extract the parameters for the VBIC model. The thermal behavior of a Si BJT is also investigated and modeled. Simulation results of extracted VBIC model are compared with the measurement data and shows very good agreement in both DC and s-parameters prediction.

1 Introduction

The Gummel-Poon model has remained essentially unchanged for over 20 years. However, the approximations that underlie the Gummel-Poon model ignore the effects that are important for accurate modeling of today' s BJT' s. For examples, parasitic transistor, avalanche multiplication, self-heating are not modeled, collector resistance modulation is ignored, and the simplified Early effect model is inaccurate. In 1995, a group of representatives from the integrated circuit and computer-aided design industries have collaborated and developed a new industry standard bipolar model called the vertical bipolar inter-company model (VBIC) to overcome these problems[1-2]. This paper presents an accurate and efficient methodology to extract the parameters for the VBIC model.

2 VBIC Model Overview

Figure 1 shows the equivalent circuit for the VBIC model[1]. The model includes an intrinsic BJT (npn used here) based on the Gummel-Poon model, and a parasitic BJT (pnp), modeled with a partial Gummel-Poon model. Quasi-saturation is modeled with the elements R_{CI}, Q_{bcx}, and a modified Q_{bc}, and by including the elements I_{bex} and Q_{bex}, along with R_{BI}, I_{be} and Q_{be}. The distributed nature of the base is modeled to a first order. Excess phase is modeled through a second order network. A weak avalanche current I_{gc} is included for the base-collector junction. The constant capacitances CBEO and CBCO are included to model extrinsic parasitic capacitances. The intrinsic base resistances, R_{BI} and R_{BIP}, are modulated by the normalized base charges, q_b and q_{bp}, respectively. The intrinsic collector resistance, R_{CI}, is modulated by V_{bci}. Finally, self-heating is modeled by including the effects of a local temperature rise on the branch constituent relationships for each network element and adding a thermal network to model the local temperature rise.

3 Parameters Extraction and Optimization

In this paper, the VBIC model was extracted for the 0.6μm×96μm (32μm×3) Si BJT using HP ICCAP modeling framework. All measurements were made with Cascade microwave probes in G-S-G (Ground-Signal-Ground) configurations. The SOLT calibration was performed before two-port s-parameter measurements to set the reference planes on the probe heads. The parasitics associated with the metal pads were removed by measuring both the dummy (metal without device) and the device and subtracting one result form the other in the y-domain. Figure 2 shows the flowchart of the VBIC parameters extraction and optimization procedure proposed in this study. Non-optimized sequence will result in less accurate extracted parameters. The steps for extracting and optimizing VBIC parameters are listed and discussed as follow.

3.1 Junction Capacitance Parameters

The first step is to extract space charge capacitance parameters because the base charge is the basic relationship of the VBIC model. Forward bias junction capacitance data should be included, up to

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where the diffusion capacitance becomes non-negligible, to ensure good extraction of the junction built-in potentials. Separation of CJC and CJEP, for the depletion components of Q_{bep} and Q_{bc}, respectively, is based on layout or extractions from different geometries.

3.2 Early Effect Parameters

The next step is to calculate the Early effect parameters from forward and reverse output characteristics based on the junction capacitance parameters extracted in the previous section. This is the major difference with respect to parameter extraction for the Gummel-Poon model, where the Early voltages come from DC data only.

3.3 Parasitic Resistors

The parasitic resistors R_{BX}, R_E, R_{CX} are determined from the flyback measurements. The R_S and R_{BP} are determined from the reverse Gummel plot of the parasitic pnp transistor. The inner base resistance R_{BI} is obtained using the input-impedance-circle method. Initial extracted resistances are thus refined by simultaneous optimization of AC and DC data.

3.4 Thermal Resistance

The rise in the device junction temperature is related to the total power dissipated in the transistor. The dissipated power P_T(W) is measured from I-V curves of the devices and given by $P_T=I_BV_{BE}+I_CV_{CE}$. The rise in junction temperature is then calculated using $T_j=P_TR_{TH}+T_0$, where T_0 is the reference room temperature[3]. The thermal resistance R_{TH} is related to the generated heat, which will be dissipating through the Si substrate. Because recombination and avalanche effects in the base current characteristic are easier to de-embed than the Early or Kirk effects in the collector current. The base current is normally used rather than collector current in extracting R_{TH}. From I-V characteristics of transistors, the thermal resistance can be extracted by[4]

$$R_{TH} = \frac{T_j^2 k}{E_{g,e} - qV_{BE} + 3T_j k - \alpha_\beta T_j^2 k} \cdot \frac{d}{dP_T}\left(\ln \frac{I_B(T_j)}{I_B(T_0)}\right) \tag{1}$$

where α_β is the relative temperature coefficient of the forward current gain β, and $I_B(T_0)$ is the base current at 300K.

In determining the thermal resistance, a DC measurement is done to obtain I_C and I_B with V_{CE} varying in the range of V_{BE} and BV_{CEO}. After de-embedding the effect of series resistances, the thermal resistance is calculated from Eqn.(1), or by simultaneous optimization of series resistances and thermal resistance to refine the values. From the extraction procedure, the parameter value of R_{TH} is 288°C/W for the Si BJT. We use this value as the thermal resistance in the thermal network of a VBIC model (Fig. 1) and ignore the thermal capacitance.

3.5 Diode Resistors

The saturation currents, emission coefficients for all transport and diode-like currents are estimated from low bias data and then refined by optimization from Gummel-Poon measurement The DC parameters of the parasitic transistor are extracted from substrate measurement. The knee currents are determined from analysis of forward, reverse, and substrate DC current gains. All these parameters can be further refined using optimization.

3.6 Quasi-saturation and Saturation Region

The quasi-saturation parameters are calculated and opotimized from the forward output characteristics under quasi-saturation and saturation operation.

3.7 Weak Avalanche Breakdown

The weak avalanche breakdown parameters are extracted and optimized based on the output characteristics in avalanche breakdown region.

3.8 Transit Time Parameters

Transit time parameters and excess phase are likewise extracted using existing techniques similar to Gummel-Poon model and then refined as part of the simultaneous DC and AC optimization.

3.9 Overall Parameters Optimization

Finally, all modeling setups should be re-simulated and fine-tuned using optimization very carefully to get the most accurate DC and AC performance prediction.

4 Modeling Results

Figures 3 and 4 compare the measurement and simulation results of the current-voltage characteristics under forward operation. As shown in Figs.3 and 4, the simulation results including self-heating effect are in very good agreement with the measurements, even at high bias region. On the other hand, the simulation results are less accurate at high bias regime without self-heating effect. We can also find that the DC predictions of the VBIC model are still very accurate under quasi-saturation operations. Figure 5 shows S11 and S22 traces under various bias conditions from the measurement and from the VBIC model with electro-thermal modeling for V_{BE} = 0.8V, 1V at V_{CE} = 2V. Figure 6 illustrates the measured and simulated magnitude of H21 versus frequency at the same bias as in Fig.5. Figure 7 shows the relationship of cutoff frequency f_T and the collector current I_C at V_{CE} = 1V, 2V and 3V from the measurement and from VBIC model. From the above results, we can conclude that the extraction methodology presented in this study is very adequate for modern BJT modeling using VBIC model.

5 Conslusions

In this paper, we present an accurate and efficient methodology to extract the parameters for the new industry standard bipolar model called the vertical bipolar inter-company model (VBIC). Simulation of extracted VBIC model shows very good results in both DC and s-parameters prediction. The simulation results shows that the VBIC model can overcome the problem that the decrease in accuracy obtained from the Gummel-Poon model in modern BJT modeling.

References

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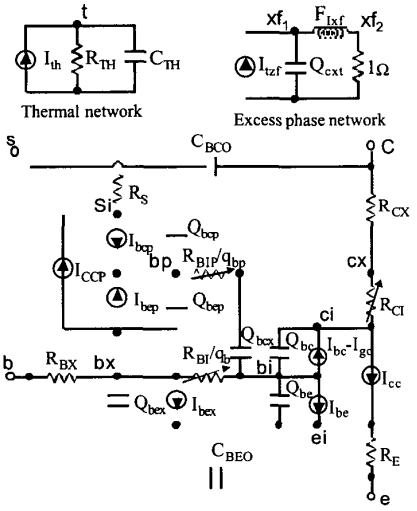


Fig.1 Equivalent circuit of the new industry standard VBIC model

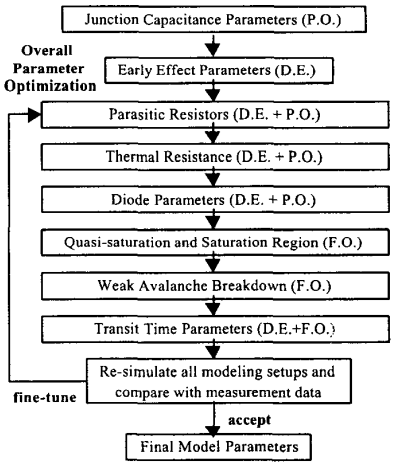


Fig.2 Flowchart for VBIC model parameters extraction and optimization.(D.E.: Direct Extraction, P.O.: Partial Optimization, F.O.: Fully Optimization)

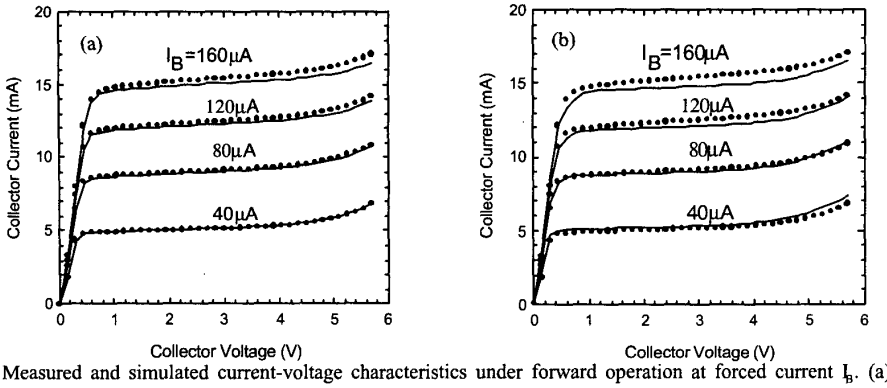


Fig.3 Measured and simulated current-voltage characteristics under forward operation at forced current I_B. (a) VBIC model with electro-thermal modeling, (b) VBIC model without electro-thermal modeling.

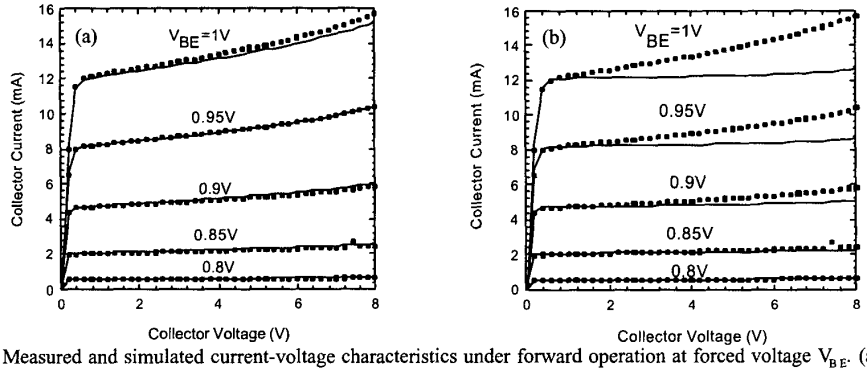
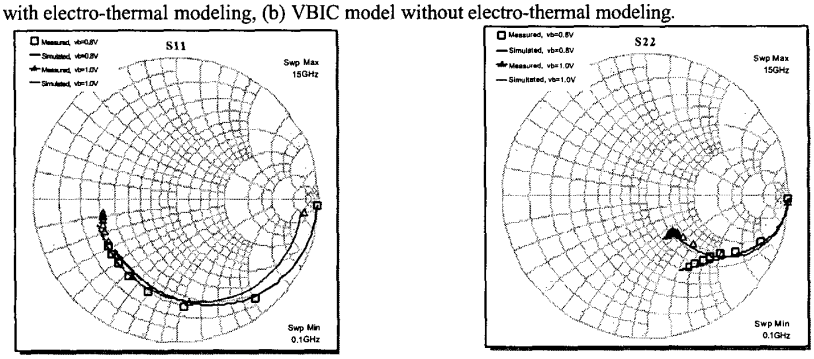


Fig.4 Measured and simulated current-voltage characteristics under forward operation at forced voltage V_{BE}. (a) VBIC model with electro-thermal modeling, (b) VBIC model without electro-thermal modeling.



(a) (b)

Fig.5 (a) S11 and (b) S22 traces at V_{BE}=0.8V, 1.0V and V_{CE}=2V from the measurement and from the VBIC model.

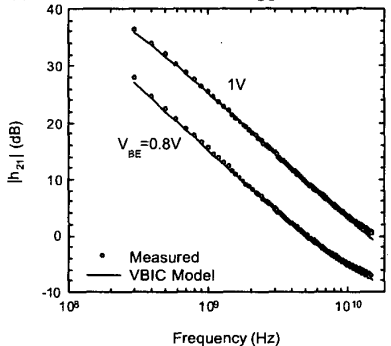


Fig.6 The magnitude of H21 versus frequency from the measurement and from the VBIC model for V_{BE} = 0.8, 1.0V at V_{CE} = 2V.

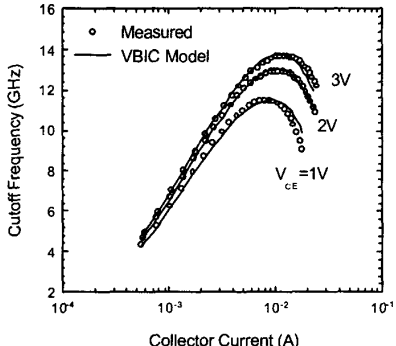


Fig.7 The relationship of cutoff frequency f_T and the collector current I_C at V_{CE} = 1V, 2V and 3V from the measurement and from VBIC model.